CLAIMS

What is claimed is:

1. A semiconductor die carrier comprising:

a radiation shielding base having a radiation shielding integrated base flange extending orthogonally from an upper surface of said base, said integrated base flange having an upper surface;

a substrate disposed on said radiation shielding base and around said integrated base flange, said substrate having an uppermost tier having an upper surface that is not higher than said upper surface of said integrated base flange; and

a radiation shielding seal lid having a radiation shielding integrated seal lid flange, said radiation shielding integrated seal lid flange having a lower surface disposed on said upper surface of said uppermost tier of said substrate.

2. A semiconductor die carrier as in claim 1 wherein said upper surface of said uppermost tier is lower than said upper surface of said integrated base flange.

3. A semiconductor die carrier as in claim 2 wherein said upper surface of said uppermost tier is lower than said upper surface of said integrated base flange by at least 0.05 millimeter.

4. A semiconductor die carrier as in claim 1 further including:

a semiconductor die disposed in a cavity formed by said radiation shielding base and said radiation shielding integrated base flange, said semiconductor die having an upper surface that is not higher than said upper surface of said integrated base flange.

5. A semiconductor die carrier as in claim 4 wherein said upper surface of said semiconductor die is lower than said upper surface of said integrated base flange.

6. A semiconductor die carrier as in claim 5 wherein said upper surface of said semiconductor die is lower than said upper surface of said integrated base flange by at least 0.05 millimeter.

7. A semiconductor die carrier as in claim 1 further including:

a semiconductor die disposed in a cavity formed by said radiation shielding base and said radiation shielding integrated base flange;

a plurality of conductive tabs disposed on said uppermost tier;

a plurality of conductive wires connected between said semiconductor die and said plurality of conductive tabs;

a plurality of conductive paths formed in said substrate and electrically coupled to said plurality of conductive tabs; and

a plurality of conductive leads disposed on an outer edge of said substrate and electrically coupled to said plurality of conductive paths formed in said substrate.

8. A semiconductor die carrier as in claim 7 wherein each of said plurality of conductive paths has a first electrically conductive via disposed in said substrate, a second electrically conductive via disposed in said substrate, and an electrically conductive line disposed in said substrate electrically coupled between said first electrically conductive via and said second electrically conductive via.

9. A semiconductor die carrier as in claim 1 wherein said substrate has a plurality of tiers, and further including:

a semiconductor die disposed in a cavity formed by said radiation shielding base and said radiation shielding integrated base flange;

a plurality of conductive tabs disposed on said plurality of tiers;

a plurality of conductive wires connected between said semiconductor die and said plurality of conductive tabs;

a plurality of conductive paths formed in said substrate and electrically coupled to said plurality of conductive tabs; and

a plurality of conductive leads disposed on an outer edge of said substrate and electrically coupled to said plurality of conductive paths formed in said substrate.

10. A semiconductor die carrier as in claim 9 wherein each of said plurality of conductive paths has a first electrically conductive via disposed in said substrate, a second electrically conductive via disposed in said substrate, and an electrically conductive line disposed in said substrate electrically coupled between said first electrically conductive via and said second electrically conductive via.

11. A semiconductor die carrier as in claim 1 wherein said substrate is formed from ceramic.

12. A semiconductor die carrier as in claim 1 wherein said radiation shielding base and said radiation shielding integrated base flange are formed from copper tungsten (CuW).

13. A semiconductor die carrier as in claim 1 wherein said radiation shielding seal lid and said radiation shielding integrated seal lid flange are formed from copper tungsten (CuW).

14. A semiconductor die carrier comprising:

a radiation shielding base having a radiation shielding integrated base flange extending orthogonally from an upper surface of said base, said integrated base flange having an upper surface;

a substrate disposed on said radiation shielding base and around said integrated base flange, said substrate having an uppermost tier having an upper surface; and

a radiation shielding seal lid having a radiation shielding integrated seal lid flange, said radiation shielding integrated seal lid flange having a lower surface that is not higher than said upper surface of said integrated base flange and is disposed on said upper surface of said uppermost tier of said substrate.

15. A semiconductor die carrier as in claim 14 wherein said lower surface of said radiation shielding integrated seal lid flange is lower than said upper surface of said integrated base flange.

16. A semiconductor die carrier as in claim 15 wherein said lower surface of said radiation shielding integrated seal lid flange is lower than said upper surface of said integrated base flange by at least 0.05 millimeter.

17. A semiconductor die carrier as in claim 14 further including:

a semiconductor die disposed in a cavity formed by said radiation shielding base and said radiation shielding integrated base flange, said semiconductor die having an upper surface that is not higher than said upper surface of said integrated base flange.

18. A semiconductor die carrier as in claim 17 wherein said upper surface of said semiconductor die is lower than said upper surface of said integrated base flange.

19. A semiconductor die carrier as in claim 18 wherein said upper surface of said semiconductor die is lower than said upper surface of said integrated base flange by at least 0.05 millimeter.

20. A semiconductor die carrier as in claim 14 further including:

a semiconductor die disposed in a cavity formed by said radiation shielding base and said radiation shielding integrated base flange;

a plurality of conductive tabs disposed on said uppermost tier;

a plurality of conductive wires connected between said semiconductor die and said plurality of conductive tabs;

a plurality of conductive paths formed in said substrate and electrically coupled to said plurality of conductive tabs; and

a plurality of conductive leads disposed on an outer edge of said substrate and electrically coupled to said plurality of conductive paths formed in said substrate.

21. A semiconductor die carrier as in claim 20 wherein each of said plurality of conductive paths has a first electrically conductive via disposed in said

substrate, a second electrically conductive via disposed in said substrate, and an electrically conductive line disposed in said substrate electrically coupled between said first electrically conductive via and said second electrically conductive via.

22. A semiconductor die carrier as in claim 14 wherein said substrate has a plurality of tiers, and further including:

a semiconductor die disposed in a cavity formed by said radiation shielding base and said radiation shielding integrated base flange;

a plurality of conductive tabs disposed on said plurality of tiers;

a plurality of conductive wires connected between said semiconductor die and said plurality of conductive tabs;

a plurality of conductive paths formed in said substrate and electrically coupled to said plurality of conductive tabs; and

a plurality of conductive leads disposed on an outer edge of said substrate and electrically coupled to said plurality of conductive paths formed in said substrate.

23. A semiconductor die carrier as in claim 22 wherein each of said plurality of conductive paths has a first electrically conductive via disposed in said substrate, a second electrically conductive via disposed in said substrate, and an electrically conductive line disposed in said substrate electrically coupled between said first electrically conductive via and said second electrically conductive via.

24. A semiconductor die carrier as in claim 14 wherein said substrate is formed from ceramic.

25. A semiconductor die carrier as in claim 14 wherein said radiation shielding base and said radiation shielding integrated base flange are formed from copper tungsten (CuW).

26. A semiconductor die carrier as in claim 14 wherein said radiation shielding seal lid and said radiation shielding integrated seal lid flange are formed from copper tungsten (CuW).

27. A method for forming a semiconductor die carrier including steps of:

machining a shielding metal base with an integrated shielding metal base flange having an upper surface;

forming a ceramic substrate from green sheets that are processed and then laminated;

affixing said ceramic substrate to said shielding metal base and around said shielding metal integrated base flange;

machining a shielding metal seal lid with an shielding metal integrated seal lid flange having a lower surface; and

affixing said shielding metal seal lid to said ceramic substrate so that said lower surface of said integrated shielding metal seal lid flange is not higher than said upper surface of said integrated shielding metal base flange.

28. A method as in claim 27, wherein the step of forming a ceramic substrate from green sheets further includes the steps of:

forming a plurality of conductive paths on said green sheets;

forming a plurality of first conductive vias and a plurality of second conductive vias in said green sheets that are electrically coupled to said conductive paths;

disposing a plurality of electrically conductive tabs on tiers formed in said substrate that are adjacent said integrated shielding metal base flange and are electrically coupled to said first plurality of conductive vias; and

disposing external bond terminals on an outer edge of said substrate that are electrically coupled to said second plurality of conductive vias.

30. A method as in claim 29, further including the steps of:

disposing a semiconductor die within a cavity formed by said shielding metal base and said integrated shielding metal base flange; and

wiring said semiconductor die to said plurality of electrically conductive tabs.

31. A method as in claim 27, further including the step of:

nickel plating said shielding metal base and said integrated shielding metal base flange after said affixing of said ceramic substrate to said shielding metal base and around said shielding metal integrated base flange.

32. A method as in claim 27, further including the step of:

nickel plating said shielding metal seal lid and said integrated metal seal lid flange after said machining step of said shielding metal seal lid and said integrated shielding metal seal lid flange.

33. A method as in claim 27, wherein the step of affixing said ceramic substrate to said shielding metal base and around said integrated shielding metal base flange further includes the steps of:

loading said ceramic substrate into an alignment tool;

applying a braze material to a portion of said ceramic substrate that will be attached to said shielding metal base;

loading said shielding metal base into said alignment tool; and

brazing said ceramic substrate and said shielding metal base in a cofire furnace.

34. A method as in claim 33, wherein said brazing material is silver copper (AgCu).

35. A method as in claim 27, wherein the step of affixing said shielding metal seal lid to said ceramic substrate further includes the steps of:

applying a layer of adhesive material to said lower surface of said integrated shielding metal seal lid flange;

disposing said shielding metal seal lid on said ceramic substrate; and

placing said shielding metal seal lid and said ceramic substrate in a nitrogen gas furnace.

36. A method as in claim 35, wherein said adhesive material is AuSn.